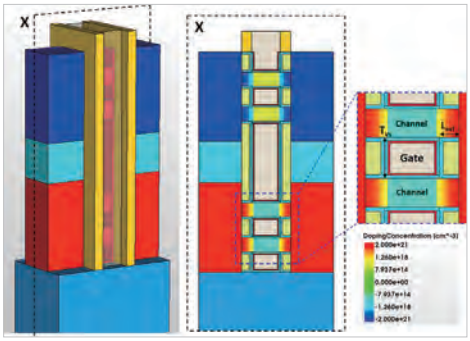
ACHIEVEMENTS

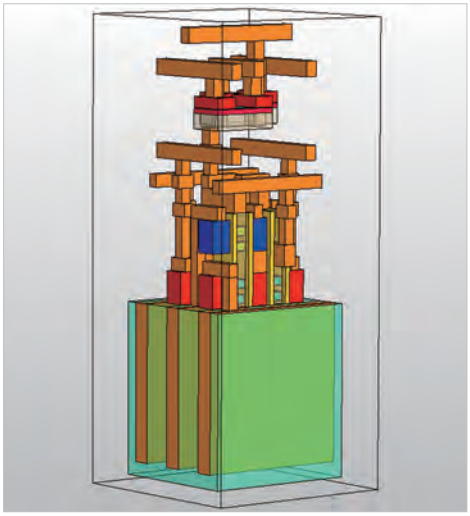
Advancing Memory Technology: Energy-Efficient CFET-based 8T SRAM

As data-centric applications, such as high-performance computing (HPC) and artificial intelligence (AI), continue to shape cutting-edge technologies, the demand for high energy efficiency becomes paramount. Such applications rely heavily on high-capacity embedded static random-access memory (SRAM) arrays that operate at low supply voltage, requiring large memory capacity and minimal SRAM cell area to boost computing capabilities. Since computing cores continually access on-chip SRAM caches, the key to making future advances in high-performance computing applications will be to enhance the density, performance, and energy efficiency of SRAM caches. Complementary Field Effect Transistor (CFET) technology, achieved by the vertical stacking of n-type and p-type transistors, has marked a significant leap in eliminating the scaling barrier and advancing SRAM density scaling. Despite the success of the 6T CFET SRAM in sustaining the scaling trend, the challenge of achieving a lower minimum operation voltage (Vmin) has been daunting due to the limitation of sharing the same read/write port.



The schematic of CFET includes two stacked nanosheets for bottom-tier n-type transistors and top-tier p-type transistors, respectively.

A research team led by Prof. Vita Pi-Ho Hu recently introduced an energy-efficient CFET-based 8T SRAM, presented at the preeminent IEEE International Electron Devices Meeting (IEDM). Their novel CFET-based 8T SRAM combines front-end-of-line (FEOL) CFET and back-end-of-line (BEOL)-compatible transistors, integrating BEOL-compatible transistors with low thermal budgets facilitates monolithic 3D integration, and opening up new horizons for System-on-Chip (SoC) scaling. The proposed CFET-based 8T SRAM offers a compelling advantage: it significantly reduces SRAM cell area as compared to the state-of-the-art Fin field-effect-transistor (FinFET) SRAM. Moreover, it eliminates read/write conflicts and enhances read stability by separating the read and write ports. This transistor strength optimization further improves write stability, eliminating the need for write assist-circuit energy overhead.

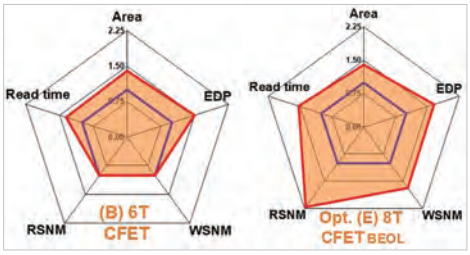


The 3D structures for the proposed CFET-based 8T SRAM.

Through meticulous design and optimization, the energy-efficient CFET-based 8T SRAM showcases remarkable advances in SRAM area scaling, speed, stability, and overall energy efficiency as compared to other CFET-based SRAMs. This optimized solution excels in every respect, opening a clear path toward energy-efficient computing for data-centric and high-throughput applications.

With its groundbreaking characteristics, the CFET-based 8T SRAM is poised to revolutionize memory technology. It offers an ideal solution for future data-centric computing needs, where performance and energy efficiency are paramount concerns.

Click or Scan the QR code to read the journal article in *IEEE Access*.



Comparisons of CFET-based 6T and 8T SRAM cells. The radar plot indicates the degree of improvements compared to 6T nanosheet (NS) SRAM (blue line in the radar plot). A larger orange area in the radar plot is better, which means more significant improvements. The proposed CFET-based 8T SRAM (opt. (E) 8T CFETBEOL) SRAM shows 2.2X and 1.7X improvements in read and write stability (RSNM and WSNM). The read time, energy-delay product (EDP) and SRAM area are improved by 53.3%, 65.7%, and 40%.

NATIONAL TAIWAN UNIVERSITY
+886-2-3366-2577
No.1, Sec. 4, Roosevelt Road Taipei, 10617 Taiwan
ntuhighlights.ntu.edu.tw

National Taiwan University 國立臺灣大學