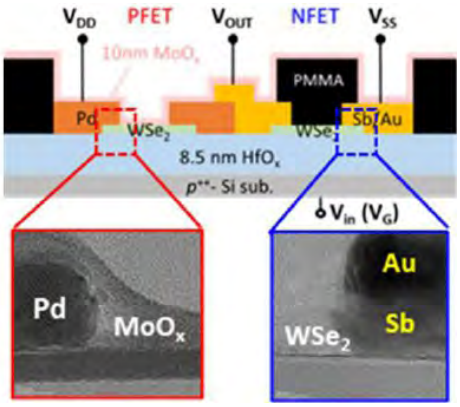
ACHIEVEMENTS

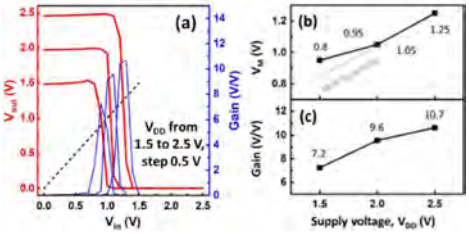
Low-Power CMOS Inverter Based on Monolayer 2D Materials

A collaborative research effort between National Taiwan University (NTU) and Taiwan Semiconductor Manufacturing Company (TSMC) has led to the successful demonstration of a low-power complementary metal–oxide–semiconductor (CMOS) inverter, constructed using monolayer two-dimensional (2D) materials. Operating under a supply voltage (V_{DD}) of 1 V, the inverter achieves precisely matched threshold voltages (V_{TH}) for both the NMOS and PMOS transistors, which is necessary for balanced switching and low static power consumption. This achievement showcases the promising feasibility of applying transition metal dichalcogenides (TMDs), such as WSe_2 and MoS_2, in the development of next-generation low-power and ultra-scaled logic integrated circuits.



Schematic diagram of the Planar homo-channel WSe_2 inverter, and the cross-sectional TEM images of n/p contact region.

To overcome the intrinsic material and fabrication challenges associated with using atomically thin semiconductors, the team conducted a thorough and systematic analysis of key process sensitivities. These included variations in monolayer transfer quality, the influence of thermal annealing on interface states, and the impact of the different wet chemical treatments used. By carefully optimizing each step—especially contact engineering and interfacial control—the researchers were able to suppress off-state leakage, reduce subthreshold swing (SS), and achieve stable enhancement-mode operation in both n- and p-type field-effect transistors (FETs).



(a) Voltage transfer characteristics (VTC) and voltage gain of a homo-channel WSe_2 inverter at various supply voltages (VDD).
(b) transition voltage (VM), defined as the point where Vout = Vin, and (c) voltage gain extracted at several VDD.

Two distinct CMOS inverter architectures were designed and fabricated. The first one utilized a homogeneous channel, employing WSe_2 for both NMOS and PMOS devices. The second one adopted a heterogeneous configuration, combining MoS_2 for NMOS with WSe_2 for PMOS to achieve unipolar conduction characteristics in each device. Although both inverters exhibited logic functionality, the hetero-channel implementation significantly outperformed its homogeneous counterpart. It delivered a peak voltage gain of 13.8 V/V, robust noise margins exceeding 80%, and a remarkably low average static power consumption rate of approximately 7 picowatts—all under sub-1V operation. These metrics mark a substantial improvement over previous 2D CMOS demonstrations.

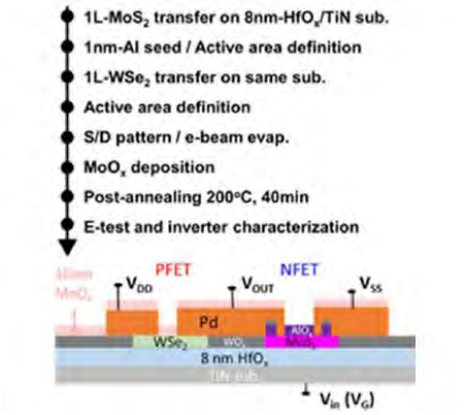
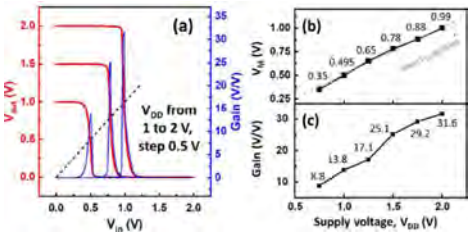


Diagram and process flow of integrated monolayer MoS_2 NMOS and WSe_2 PMOS hetero-channel inverter.

Beyond the basic electrical performance, this work also validates the critical role of integrated process co-optimization in 2D logic technologies. The study establishes an important benchmark, demonstrating that scalable, high-efficiency CMOS logic

circuits based on monolayer TMDs can be reliably implemented through tailored fabrication strategies.

This research was presented at the 2024 IEEE International Electron Devices Meeting (IEDM). The NTU contributors gratefully acknowledge support from the TSMC-NTU Joint Research Center and the National Science and Technology Council, Taiwan.



(a) VTCs and voltage gain of a MoS_2/WSe_2 hetero-channel inverter at various VDD. (b) VM and (c) voltage gain as a function of VDD.

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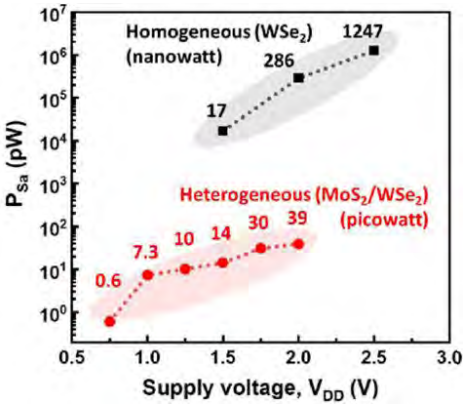

Comparison of the average static power versus VDD for both homo- and hetero-channel inverters.

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