

TEACHING & LEARNING

NTU Advances 2D Semiconductor Technologies at IEEE VLSI 2026

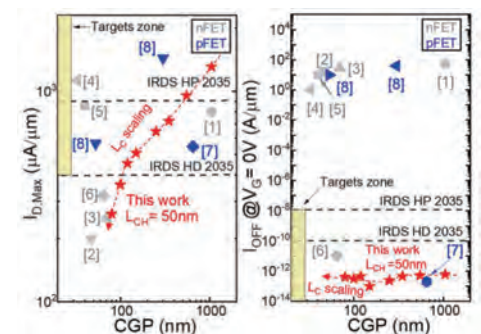
Share:     



Presentation by the TSMC research team at the 2026 IEEE Symposium on VLSI Technology and Circuits. The research was carried out through close collaboration among National Taiwan University (NTU), The University of Tokyo (UTokyo), and the National University of Singapore (NUS).

The IEEE Symposium on VLSI Technology and Circuits (IEEE VLSI) is one of the world's premier conferences in semiconductor research, where leading companies and research institutes present their latest technological innovations. This year, major semiconductor manufacturers, including TSMC, Intel, and Samsung, showcased their latest technology roadmaps. Among them, TSMC introduced its A16 technology, featuring Super Power Rail (SPR) backside power delivery to further improve power efficiency and performance. As conventional silicon devices approach their physical scaling limits, two-dimensional (2D) semiconductors have attracted increasing attention as promising candidates for next-generation electronics because of their atomically thin structure and excellent electrical properties.

Researchers from Professor Chih-I Wu's Laboratory at National Taiwan University (NTU) participated in three collaborative studies presented at IEEE VLSI 2026. While significant progress has been made in n-type 2D transistors,

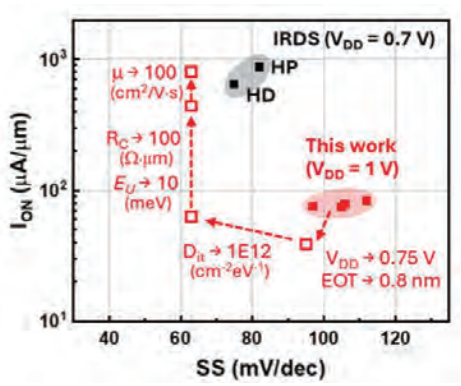


Benchmark of (a) maximum on-current ($I_{D,Max}$) and (b) off-current (I_{OFF} at $V_G = 0$ V) versus contact-gate pitch ($LC + LCH$) for reported 2D nFETs (gray symbols) and pFETs (blue symbols), demonstrating the performance of the team's device.

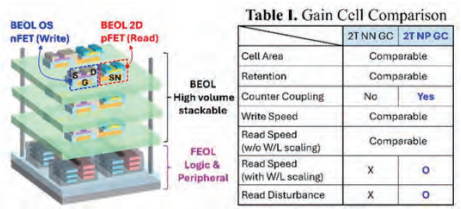
the development of high-performance p-type devices remains a key challenge for future CMOS technology. In collaboration with National Yang Ming Chiao Tung University (NYCU), The University of Tokyo (UTokyo), and the National Institutes of Applied Research (NIAR), the research team demonstrated record-setting monolayer WSe₂ p-channel transistors in the multidisciplinary field of advanced materials, surface, and contact engineering. In addition, a joint study with TSMC investigated the influence of interface defects and contact resistance on transistor performance, providing important design guidelines for future low-power integrated circuits.

Beyond transistor development, the collaboration also demonstrated the first back-end-of-line (BEOL)-compatible two-transistor gain-cell (2T GC) memory, integrating a 2D WSe₂ p-type transistor with an oxide-semiconductor n-type transistor. The proposed memory design achieved excellent read performance and scalability, confirming the potential of 2D semiconductors for future high-density memory and AI computing applications. Together, these three studies highlight the broad potential of 2D semiconductor technology, spanning fundamental device engineering, transistor optimization, and advanced memory applications.

These achievements were made possible through close collaboration among research labs at NTU, TSMC, NYCU, UTokyo, and NIAR (including TSRI and NCIR). By combining expertise in materials, device fabrication, simulation, and circuit design, the partnership continues to advance next-generation semiconductor technologies. The research team also acknowledges the long-term support of the TSMC–NTU Joint Research Center, whose collaboration has played a vital role in promoting innovative semiconductor research and strengthening Taiwan's leadership in advanced semiconductor technologies.



Projected ON-current at $V_{DD} = 0.75\text{ V}$ for monolayer WSe₂ devices with improvements in key device metrics. The current devices achieve an ON-current of approximately $80\text{ }\mu\text{A}/\mu\text{m}$ at $V_{DD} = 1\text{ V}$. Simulations project that the ON-current could reach $800\text{ }\mu\text{A}/\mu\text{m}$ at $V_{DD} = 0.75\text{ V}$ through optimized equivalent oxide thickness (EOT), interface trap density (D_{it}), Urbach energy (EU), contact resistance (RC), and hole mobility.



Schematic illustration and performance comparison of the monolithic three-dimensional integration of the 2T NP Gain-Cell (GC) memory.